REMARKS

Claims 1-19 and 21-30 are pending in this application. By this Amendment, claims 1, 2, 8, 15-16, 19 and 28 are amended to further clarify some of the already distinguishable features. Support for the amendments can be found, for example, at least at page 8, line 19 through page 10, line 26, and in Figs. 4 and 5. Claim 20 is canceled without prejudice or disclaimer. No new matter is added.

The courtesies extended to Applicant's representative by Examiner Bengzon at the July 15 interview are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below, which constitute Applicant's record of the interview.

The Office Action rejects claims 1-11, 14-18 and 28-30 under 35 U.S.C. §103(a) over Narasimhan (U.S. Patent No. 6, 446,192) in view of Bishop (U.S. Patent Number 4,914,653), and over Bishop in view of Narasimhan; and rejects claims 12, 13 and 19-27 under 35 U.S.C. §103(a) over Narasimhan in view of Bishop and further in view of Balachandran (U.S. Patent Publication No. 2005/0078620). The rejections are respectfully traversed.

As discussed during the interview, Narasimhan discloses an apparatus for connecting peripheral devices to client computers through a standard network interface, such as Ethernet using TCP/IP. Narasimhan's device is a network interface chip (NIC) that is used to relay and translate signals from the network to the peripheral device. Thus, the NIC receives a communication from the network, converts the information into data that is compatible with the peripheral device and subsequently, communicates the converted data to the peripheral device. Narasimhan, additionally, provides a path in reverse to allow the peripheral device to

communicate back to a client computer on the network. Narasimhan, however, fails to provide the claimed management port for a wireless device platform.

In particular, Narasimhan fails to disclose or render obvious a management block to receive command data from the at least one processor or peripheral through a predetermined logic channel in the inbound link, *the management block providing a corresponding command signal on the microprocessor bus system*, the command signal performing a management function for the microprocessor system, *the management block being further adapted to receive a response signal from the microprocessor bus system and the management block transmitting corresponding response data through a predetermined logic channel in the outbound link* to the at least one processor or peripheral via the inter-processor bus, as recited in independent claim 1 and similarly recited in independent claims 8, 15, 19 and 28. Narasimhan is silent on such a feature, but instead merely relays and converts network communications to the protocol used by a peripheral device.

The microprocessor bus system could be, for example, the core bus of a microprocessor. As discussed during the interview, one example of issuing command signals on the microprocessor bus system (in this example a core bus) may be if the microprocessor is hung up with processing. Such a situation would disable the ability to perform communications over the standard I/O paths, which, for example, are connected to a peripheral bus. Alternatively, the management block could receive, through a predetermined channel, command data. Subsequently, the management block could issue a command to the processor core over microprocessor bus, thus by-passing the peripheral bus. Narasimhan fails to disclose or render obvious a management block or similar device that is capable of producing such command

signals on the microprocessor bus system. Thus, Narasimhan fails to disclose or render obvious the combination of features recited by independent claims 1, 8, 15, 19 and 28.

One concern discussed during the interview was the origin of the communications and the specific paths of the inbound and outbound links. Applicant amends independent claims 1, 8, 15, 19 and 28 for further clarity, as discussed at the interview. In this regard, Applicant also submits that Narasimhan fails to disclose or render obvious the claimed *inbound link providing a path for communications from the inter-processor bus to a peripheral bus of the microprocessor subsystem*, the inbound port receiving communications from at least one processor or peripheral communicating over the inter-processor bus and *the outbound link providing a path for communications from the peripheral bus of the microprocessor subsystem to the inter-processor bus*, the outbound port transmitting communications over the inter-processor bus to the at least one processor or peripheral as recited in independent claim 1 and similarly recited in independent claims 8, 15, 19 and 28.

Bishop and Balachandran fail to cure the deficiencies of Narasimhan. In particular, both Bishop and Balachandran are silent regarding the above-mentioned features. Accordingly, whether taken in combination or considered individually, the applied references fail to disclose or render obvious the combinations of features recited by the independent claims. Thus, independent claims 1, 8, 15, 19 and 28 are patentable over the applied references. Claims 2-7 depend from independent claim 1; claims 9-14 depend from independent claim 8; claims 16-18 depend from independent claim 15; claims 20-27 depend from independent claim 19; and claims 29-30 depend from independent claim 28, and are therefore patentable over the applied references for at least the same reasons, as well as for the additional features they recite.

At least in view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of all pending claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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